CLAIMS

What is claimed is:

1. A method for accessing memory data, for providing a data storage buffer mechanism for a non-cacheable memory region in a memory unit of an electronic device, the method comprising the steps of:

having an interface unit receive a memory accessing request from a processing unit, and allowing a non-cacheable memory buffer unit to conduct a comparison to determine if there is a memory address corresponding to that in the memory accessing request, if no, forwarding the memory accessing request to an arbitration unit for accessing data in the memory unit;

having the non-cacheable memory buffer unit retrieve memory data during transmitting the data from the memory unit to the interface unit to update data stored in the non-cacheable memory buffer unit; and

having the non-cacheable memory buffer unit pre-read continuous memory address data following the retrieved data to enhance speed of accessing the continuous data for the processing unit.

2. The method of claim 1, wherein the memory data is read when there is a memory address corresponding to that in the memory accessing request.
3. The method of claim 1, wherein the electronic device is selected from the group consisting of personal computer, notebook computer, palm computer, personal digital assistant, server, and workstation.
4. The method of claim 1, wherein the memory unit is selected from the group consisting of static random access memory, dynamic random access memory, synchronous dynamic random access memory, and high-speed data-transmission synchronous dynamic random access memory.
5. The method of claim 1, wherein the processing unit is a central processing unit or microprocessor.
6. A method for accessing memory data, for providing a data storage buffer

mechanism for a non-cacheable memory region in a memory unit of an electronic device, the method comprising the steps of:

when a processing unit, apparatus or module of the electronic device writes data to the memory unit, having a non-cacheable memory buffer unit compare if a memory address of the written data is consistent with that of data stored in the processing unit, apparatus or module of the electronic device; and

when the consistency of memory address is verified, having the non-cacheable memory buffer unit update the data of the consistent memory address.

7. The method of claim 6, wherein the electronic device is selected from the group consisting of personal computer, notebook computer, palm computer, personal digital assistant, server, and workstation.
8. The method of claim 6, wherein the memory unit is selected from the group consisting of static random access memory, dynamic random access memory, synchronous dynamic random access memory, and high-speed data-transmission synchronous dynamic random access memory.
9. The method of claim 6, wherein the processing unit is a central processing unit or microprocessor.
10. The method of claim 6, wherein the apparatus is an external peripheral device or embedded peripheral device.
11. The method of claim 6, wherein the module is an external peripheral device or embedded peripheral device.
12. A system for accessing memory data, for providing a data storage buffer mechanism for a non-cacheable memory region in a memory unit of an electronic device, the system comprising:

the memory unit for storing data to be accessed by the electronic device and having the non-cacheable memory region;

an interface unit connected to a processing unit, for transmitting data between the processing unit and a unit or module of the electronic device;

a non-cacheable memory buffer unit for accessing data in the non-cacheable memory region for the unit or module of the electronic device; and

an arbitration unit for forwarding a memory accessing request to the memory unit to read data from the memory unit when the unit or module of the electronic device fails to read required data from the non-cacheable memory buffer unit.

13. The system of claim 12, wherein the electronic device is selected from the group consisting of personal computer, notebook computer, palm computer, personal digital assistant, server, and workstation.

14. The system of claim 12, wherein the memory unit is selected from the group consisting of static random access memory, dynamic random access memory, synchronous dynamic random access memory, and high-speed data-transmission synchronous dynamic random access memory.

15. The system of claim 12, wherein the processing unit is a central processing unit or microprocessor.

16. The system of claim 12, wherein the unit of the electronic device is an external peripheral device or embedded peripheral device.

17. The system of claim 12, wherein the module of the electronic device is an external peripheral device or embedded peripheral device.